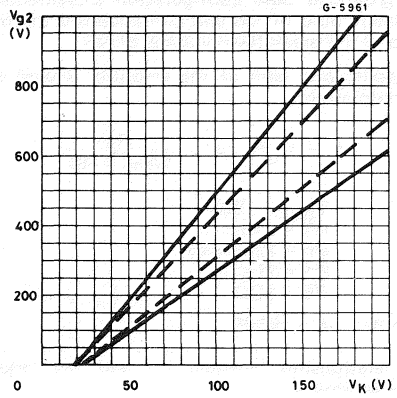
TDA8153: A MONOLITHIC RGB VIDEO AMPLIFIER

The SGS TDA8153 is a bipolar monolithic integrated circuit which includes three video amplifiers required to drive the cathodes of a colour CRT, bias circuits, a power supply for the grid 1 of the picture tube and three cathode current sensors, used for automatic cut-off control.

STATIC FEATURES

Fig. 1 shows the cut-off characteristic of a picture tube. The two full straight lines define the maximum spread for the cut-off voltage among all the picture tubes belonging to the same family. The maximum spread is 1.8/1 but when a single picture tube is analysed, which is represented by the area between the full straight line and the dotted line near it, the spread reduces to 1.2/1. The latter is therefore the cut-off adjustment range that is required in a video amplifier, assuming that the difference between the tubes is recovered by acting on the grid 2 voltage.

Fig. 1 - Cut-off characteristics of a picture tube



From fig. 2 the relationship between the V_{gK} voltage and the electron gun may be read, it is important consider that the electron gun with highest cut-off voltage also has the highest peak current. This ensures the best definition of the white peaks. The voltage values are referred to the grid 1 bias value, whose magnitude has to satisfy two conflicting requirements; it has to be as small as possible (to better limit the breakdown voltage required of the active components of the amplifier, and therefore the dissipated power) and it has to be greater than the saturation voltage of the video amplifier.

Fig. 2 - Cathode peak current vs. output voltage

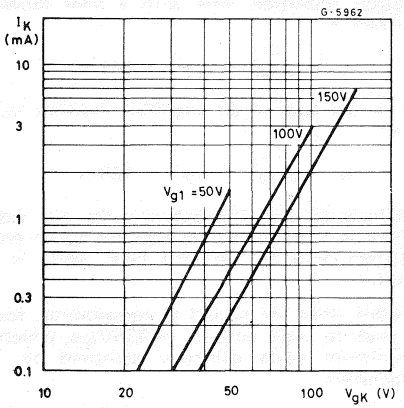
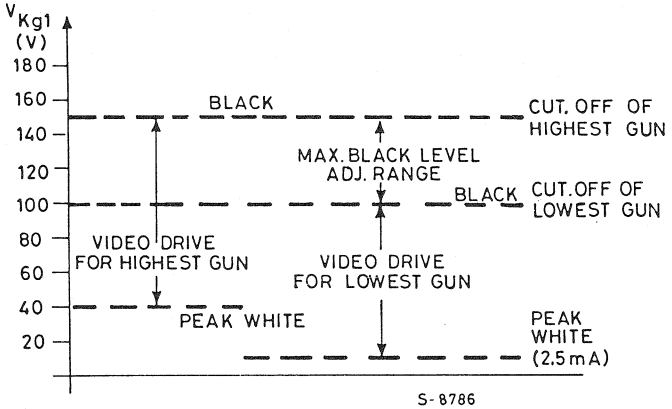


Fig. 3 shows all the components contributing to define the minimum supply voltage of the video amplifier.

Fig. 3 - Contributions to the minimum supply voltage of the TDA8153



This minimum voltage is the sum of V_{g1}, of V_{gk} referred to the lower gun, of the voltage required to recover the difference of the cut-off values and of the higher saturation voltage of the amplifier.

By executing the calculations and keeping the possible spread voltage into account, it will be found that the breakdown voltage required to the active components of the video amplifier is 250V.

DYNAMIC FEATURES

The main point related to the dynamic performance is the response to a step signal. The rise and fall time t_r and t_f must not exceed 100ns at the maximum signal amplitude and with rated load. This is essential to eliminate the coloured sides on the picture due to the tolerance of the response time of the three video amplifiers. Assuming that the generator providing the input signal to the amplifiers has, for instance, a rise time t_a = 100ns, the output transition time with a final showing t_{r1} = 100ns is:

$$t_r = \sqrt{t_a^2 + t_{r1}^2} = 141ns$$

while, in the case of an amplifier showing t_{r2} = 80ns, is:

$$t_r = \sqrt{t_a^2 + t_{r2}^2} = 128ns$$

The differential rise time between the two video amplifiers is 13ns which corresponds to an error of 0.13mm or a 26'' (67cm) tube, which is inperceptible.

The 100ns limit for t_r and t_f corresponds, for a 100V peak to peak output, to 835V/μs, which is the minimum value generally accepted by TV manufacturers.

The passband of the video amplifier, although being a less stringent requirement compared to the step response, is acquiring an increasing importance in the most recent TV color generations, due to the introduction of graphic transmission systems and to the widespread use of SCART connectors.

Normally the passband at 3dB for small signals of the video amplifier has to be at least 6MHz, with a maximum ripple of ± 1.5dB, and is generally a function of the compensations introduced on the input side.

The passband for large signals is generally limited by the bias current of the stage. Normally a minimum value of 4.5MHz is accepted.

VIDEO AMPLIFIER

Fig. 5 shows the electric diagram of a single channel of the TDA8153.

Given the required rise and fall features (slew rate about 1000V/μs), it is necessary to use a configuration able to minimize the effects of the stray capacitances and to neutralize the Miller effect. For, this reason the common base configuration is used.

In this way the collector load of Q6 is about 1/gm and, having the stage a unit gain, no Miller effect is present. The same is for Q5 that, having its base connected to V_S, reports Cμ5 without multiplying coefficient.

The grounded base configuration increments the dominant pole of Q6 and consequently the bandpass and the breakdown voltage of Q5.

The open loop gain of the amplifier is with good approximation:

$$A = V_o/V_i = - \frac{R1}{1/gm + R5}$$

Since: V_{odc} = 150V
HT = 210V
gm = 128mA/V
R1 = 21KΩ
R5 = 30Ω

it results: A = -55dB

The relationship between R1 and the required response time is:

$$R1 = \frac{1.2\ (V_{HT} - V_{odc})\ t_r}{C_{tot}\ V_{odc}}$$

were: $C_{tot} = C_{s1} + C\mu5 + C\mu1$

A typical required rise time is t_r = 85ns with an output amplitude V_{opp} = 80V; making C_{tot} = 3.5pF it follows that R1 = 21KΩ. This ensures a rise and fall time smaller than the acceptable maximum within a large variation range for the parameters.

Fig. 4 - TDA8153 semplified schematic diagram

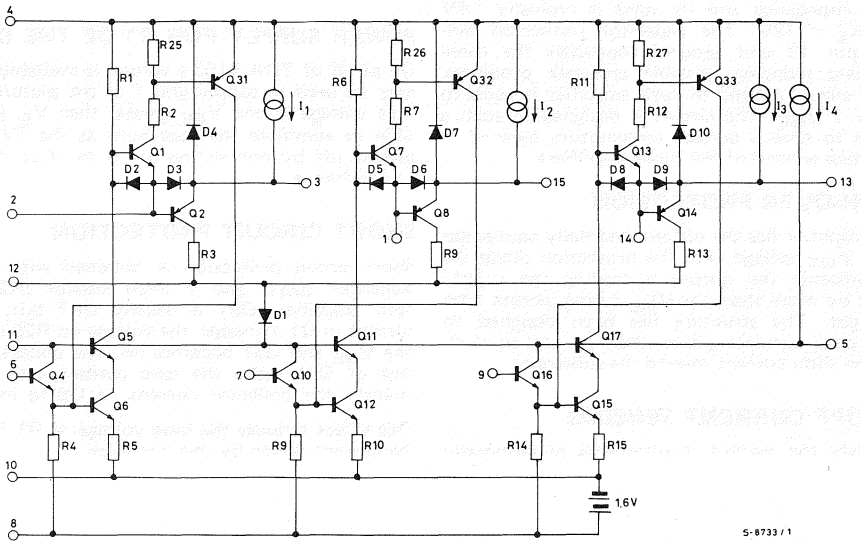


Fig. 5a - Semplified diagram for one channel

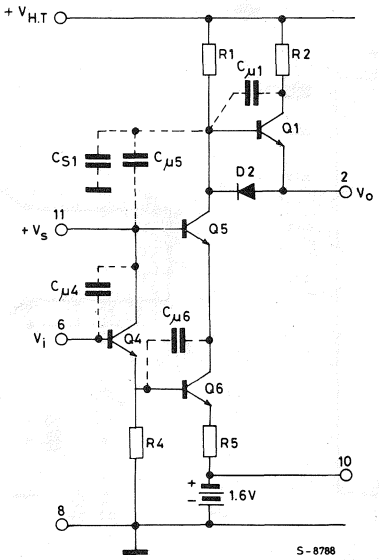
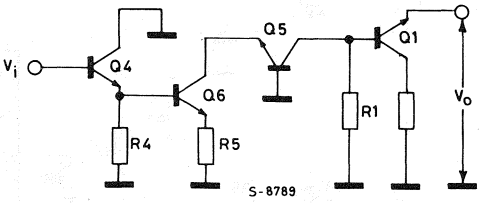


Fig. 5b - Semplified diagram for open loop gain



There are three operating conditions for the video amplifiers:

- **Stand-by condition** - In this condition Q6 and Q1 (Fig. 4) are conducting the stand-by current; Q5 current is supplied by R1 and the Q1 current flows through the feedback network. D2 doesn't conduct being reverse biased.
- **Negative-going input signal** - The signal creates a current decrease in Q5 and Q6 and, consequently, an increase in Q1 base voltage. D2 doesn't conduct and the load capacitances is charged through Q1.

- **Positive-going input signal** - In this case the load capacitance is discharged through D2 and Q5. The high open loop gain ensures a negative feedback ratio in all the applications.

VOLTAGE REFERENCE

The voltage on pin 10 is the internal reference voltage for the video amplifiers; it is provided at a low impedance and its value is typically 1.6V with V_S = 12V. The capacitor connected between pin 10 and ground decouples the three amplifiers reducing possible crosstalk problems. So the virtual ground of each amplifier is equal to V_{ref} + 2 V_{BE}. The circuit is designed in such a way as to have a perfect temperature balance of the virtual ground of the three amplifiers.

FLASH-OVER PROTECTION

Each amplifier has the output internally connected to the V_{HT} voltage with the protection diode D4 that prevents the output exceeding the supply voltage by more than one V_{BE} during picture tube discharges. The structure has been designed to accept peak currents greater than 1A and to minimize the eddy current toward the substrate.

CUT-OFF CURRENT SENSING

To satisfy the current requirements of automatic cut-off adjustment, a PNP able to sense the cathode current has been built in for each video amplifier. The availability of commercial ICs performing the sequential automatic cut-off adjustment allows the use of only one pin; each PNP is biased by a 15μA current generator. In this way, when the cut-off current of the picture tube is being measured, it is possible to automatically compensate either positive or negative leakage currents.

POWER SUPPLY FOR G1 OF THE CRT

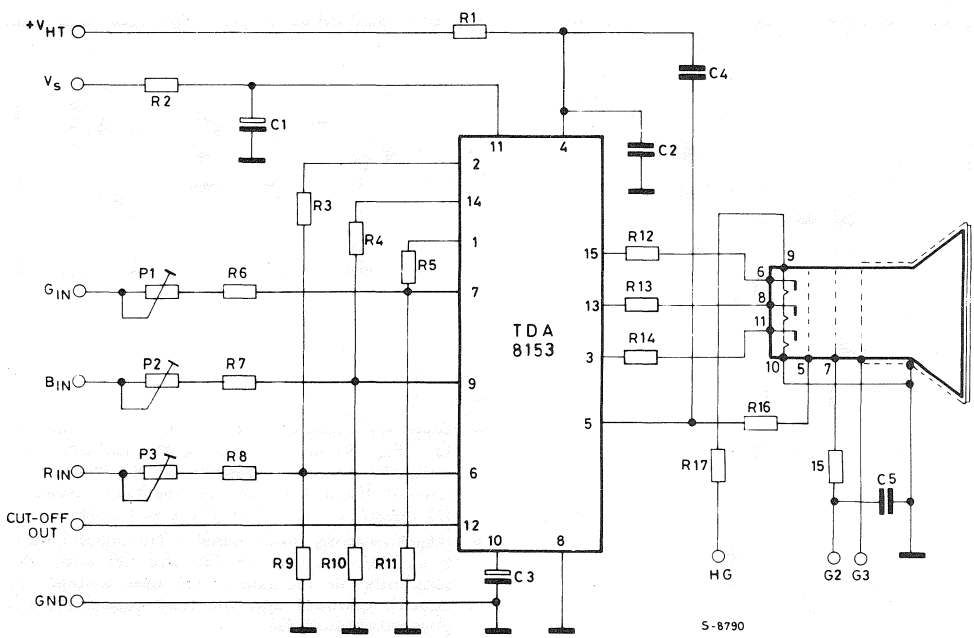
On pin 5 of TDA 8153 a voltage is available which may be used to supply grid 1 of the picture tube. This voltage is one V_{BE} greater than V_S. Its possible to eliminate the spot-burn as the TV sets is turned off by connecting pin 5 to V_{HT} through a capacitance.

SHORT CIRCUIT PROTECTION

Short circuit protection is obtained with a PNP transistor (Q31) and a small resistor (R25) for each amplifier. Q31 is usually OFF but, if the current in Q1 increases, the voltage on R25 reaches one V_{BE} and Q31 becomes on. The collector current of Q31 make the base current, and consequently the collector current of Q6 to increase.

This effect reduces the base voltage of Q1 limiting the current driven by this transistor.

Fig. 6 - Application diagram



DIMENSIONING EXTERNAL COMPONENTS (Fig. 6)

Because of the high open loop voltage gain of the amplifier, the closed loop voltage gain can be written with good approximation:

$$G = -\frac{R1}{R1 + Pg}$$

Making Pg = 0 we can find the relationship between R1, R3 and the maximum gain required in the application:

$$R1 = \frac{R3}{|G_M|}$$

With reference to fig. 5 and fig. 6 the feedback in DC gives:

$$V_{out} = (1 + R3/R1 + R3/R2)(V_{ref} + 4V_{BE}) - + R3/R1\ V_{idc} =$$

$$= (V_{ref} + 4\ V_{BE}) + R3/R1\ (V_{ref} + 4\ V_{BE} - + V_{idc}) + R3/R2\ (V_{ref} + 4\ V_{BE})$$

By expressing R2 it follows that:

$$R2 = \frac{R3\ (V_{ref} + 4\ V_{BE})}{V_{out} - V_{ref} - 4V_{BE} - R3/R1\ (V_{ref} + 4V_{BE} - V_{idc})}$$

If we assume $V_{idc} = V_{ref} + 4\ V_{BE}$:

$$R2 = \frac{R3\ (V_{ref} - 4\ V_{BE})}{V_{out} - V_{ref} - 4V_{BE}}$$

Knowing the maximum gain required for the stage and the maximum black level, which is dictated by the picture tube features, and imposing the R3 feedback resistance, the two resistances R1 and R2 may be calculated. R3 must be chosen the lowest as possible according with the maximum power accepted by the application; a good compromise is R3 = 68KΩ.

The P_1 potentiometer is in series connected to R1, to adjust the storage gain. Its value is given by:

$$P_1 = \frac{\Delta G\ R1\ 2}{R3 - R1\ \Delta G}$$

Where $\Delta G = G_M - G_m$ is the maximum range of variation of the gain.

When the application doesn't require the cut-off automatic control, a potentiometer is connected in series with R2, too, so that the black level may be adjusted.

Knowing the required ΔV_{bl} black level variation, and assuming:

$$K = \frac{\Delta V_{bl}}{V_p\ 2}$$

$$P_{bl} = R2^2\ K/(R3 + R2\ K)$$

When the cut-off automatic control is being performed there is no use in connecting the black level adjustment potentiometer. In this case the R2 value will be that corresponding to the nominal black level required by the picture tube.

The R4 and R5 resistors protect the integrated circuit during picture tube discharges. At the same time, it has to show a low value to achieve an optimum video band.

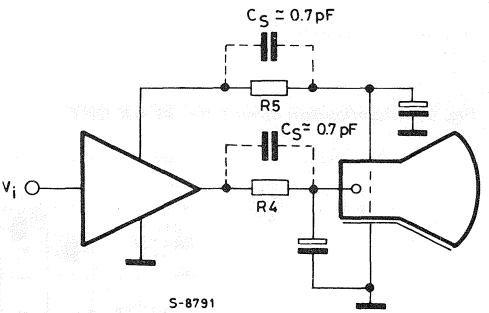
The best compromise is achieved with a resistor of about 1KΩ. As fig. 7 shows, the protection resistor is connected in parallel with the parasitic capacitor, that limits its effect. This problem may be partially solved using resistors with half watt minimum power on splitting the protection resistor in two halves.

From the experience of some picture tube manufacturers, it may be seen that compared to the amplifier against the picture tube discharges with two protection resistances in series connected increases by 25% approximately.

Similar considerations have to be made for the resistance in series connected to grid 1. In fact, R5 generally has a value with the same magnitude order of R4.

Sometimes a 100μH choke is required in series to R4 and R5 for safe the output stages from the flashover if the CRT is not a soft arc type.

Fig. 7 - Connection of protection resistors.



APPLICATION CIRCUITS

Fig. 8 and fig. 9 show TDA8153 applications for S4, S6 and 30AX CRTs, designed to be matched to the cut-off automatic control of the TDA3562A.

For proper operation of the device it is essential to connect a resistance of at least 200Ω in series to the V_{HT} power supply voltage. This allows operation with absolute confidence up to 250V even in applications where V_S may be absent in standby conditions.

The three capacitors connected in parallel with the input resistors compensate the effects of the distri-

buted constants of the printed circuit on the step response times. Their values must be selected on the basis of the lay-out and it can be considered as function of the printed circuit.

The application provides a black level of 150V and a nominal gain of 26dB. Therefore, the peak-to-peak signal with color bars at nominal saturation and maximum contrast is V_{PP}.

Fig. 8 - Application circuit for S4, S6 CRT

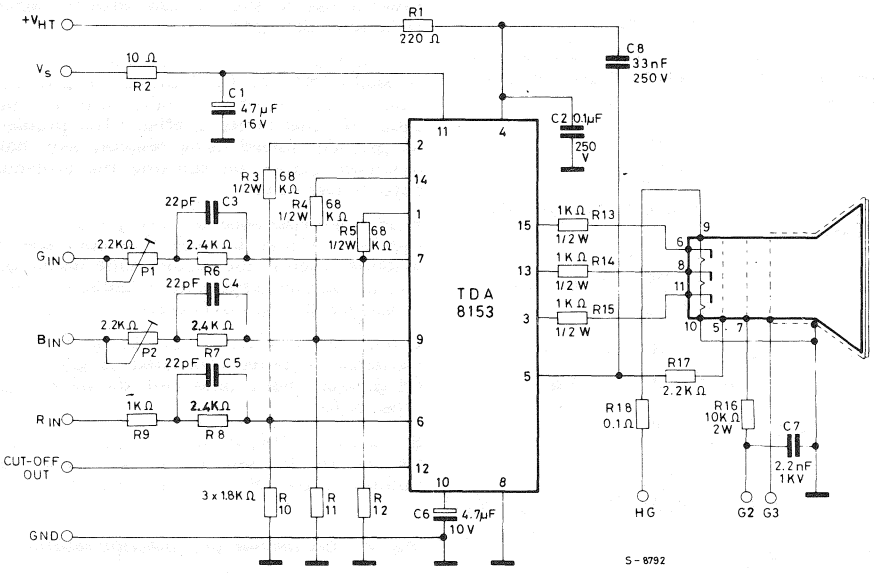


Fig. 9 - Application circuit for 30 AX CRT

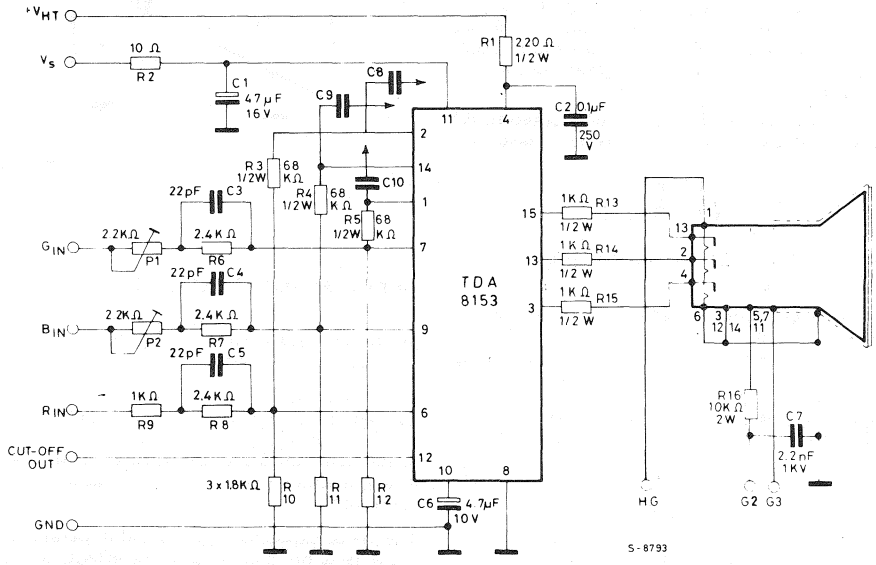


Fig. 10 and fig. 11 show the P.C. board and component lay-outs of the applications shown in fig. 8 and the 9.

Due to the small size of the printed circuit, it is possible to mount the TDA8153 directly beside the picture tube socket, to minimize the capacitances of the connections between the video amplifiers and the picture tube cathodes.

Special care has been taken in realizing the lay-out of the printed circuit to achieve the best possible symmetry of the three channels. To prevent possible oscillations problems, the connections to the three virtual grounds at the amplifier's input have been concentrated as much as possible.

Fig. 10 – P.C. board and components layout of the circuit of fig. 8 (1 : 1 scale)

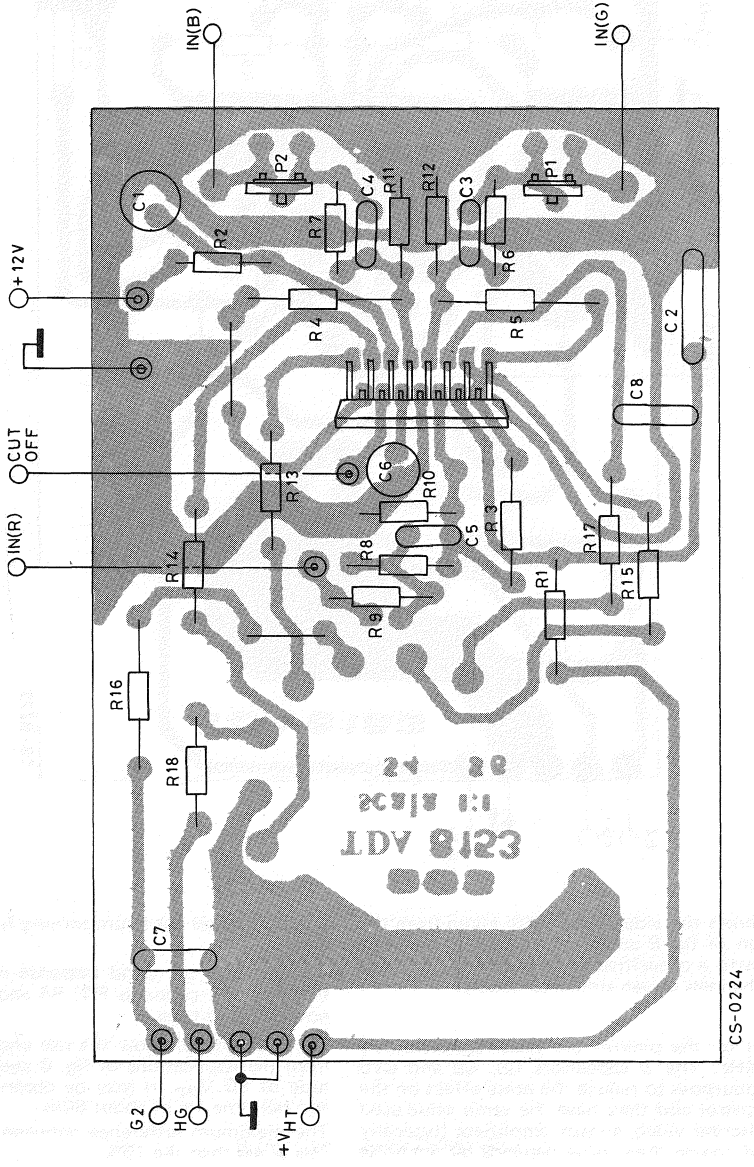
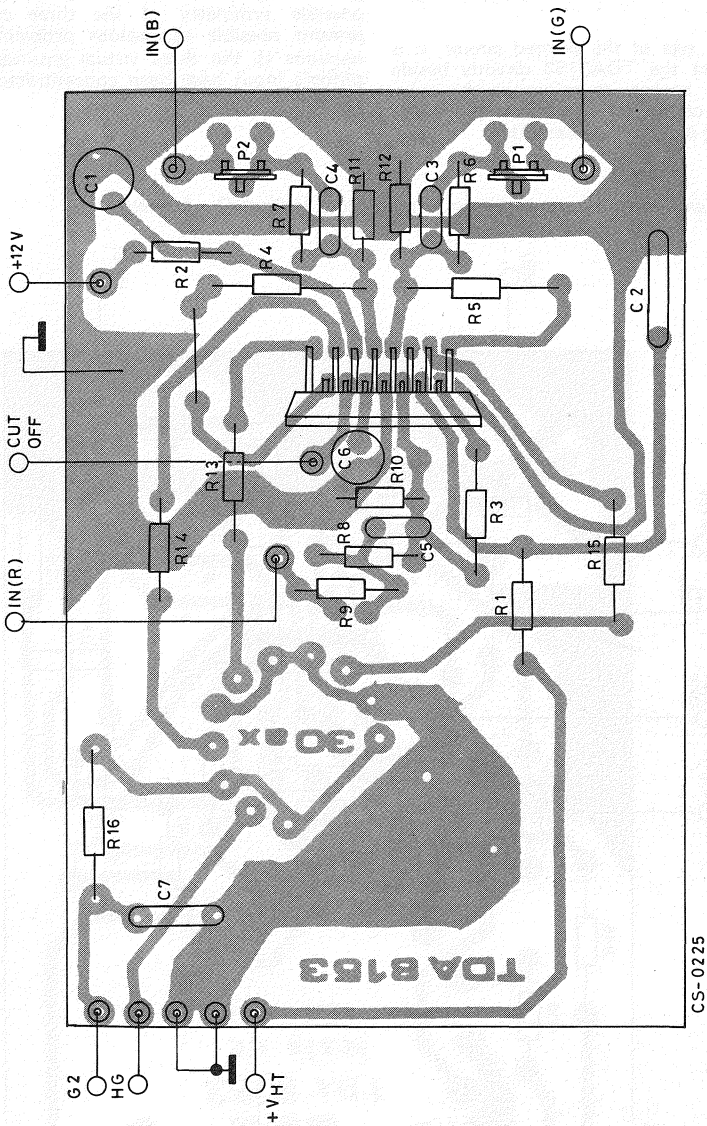


Fig. 11 - P.C. board and components layout for the circuit of fig. 9 (1 : 1 scale)



Fig, 12 shows the video bandwidth taken from the application of fig. 8 and 9 for an output signal of 80 V_{PP} with a capacitive load of about 12pF and with all channels driven simoultaneously.

As shown on the picture the video bandwidth is about 4MHz. The 3 capacitors C8, C9 and C10 have the pourpose to reduce the noise effect on the cut-off control and they have the same value used on the discrete video output amplifiers (typically 680pF) of course their value depends by the noise amplitude and spectrum coming from the IF video stage.

To optimize the band response and to minimize the crosstalk channels R3, R4 and R5 must be of not inductive type.

Fig. 3 a) and b) show the rise and fall time taken from the applications of fig. 8 and 9 for an amplitude of 80 V_{PP}. It may be observed that the rise and fall time are of about 80ns.

The maximum difference between the three channels is less than the 10%.

Fig. 12 - Video bandwidth of the TDA8153

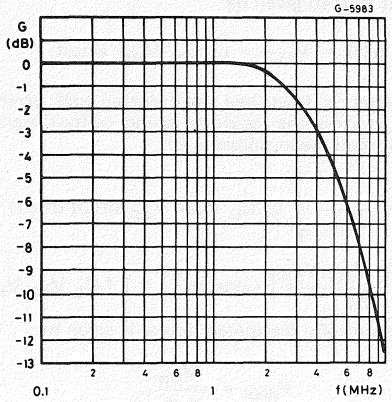
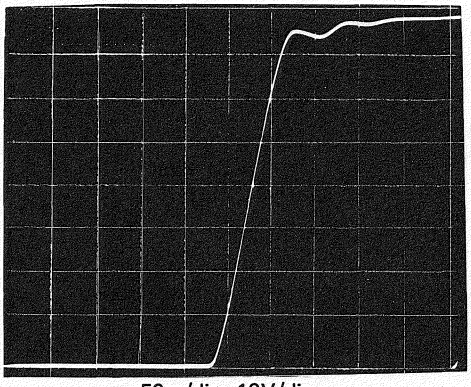
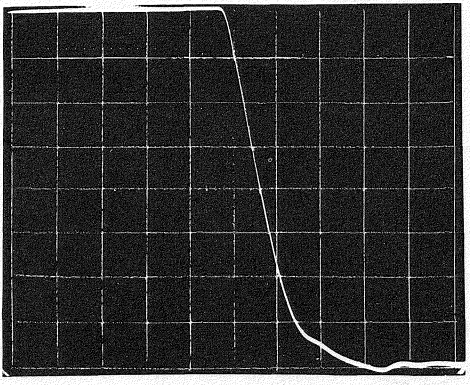


Fig. 13a - Rise time



50ns/div; 10V/div

Fig. 13b - Fall time



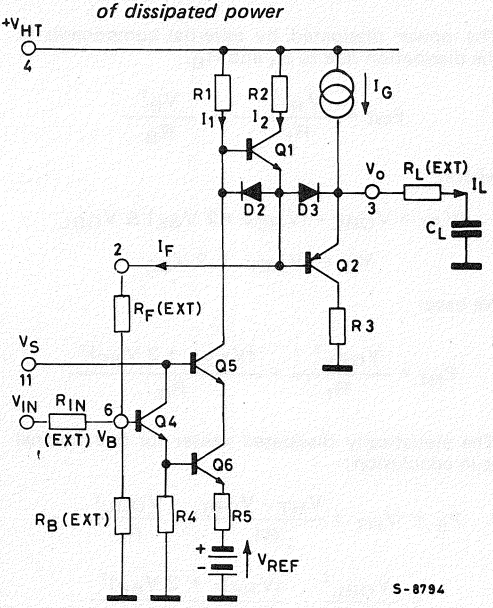
50ns/div; 10V/div

DISSIPATED POWER

The power dissipated by the video amplifier is constituted by two separate components: the static power and the dynamic power, which is a function of the signal amplitude and frequency spectrum.

The total power dissipation can be divided into static and dynamic power to simplify the cal-calculation.

Fig. 14 - Electric diagram used in the calculation of dissipated power



STATIC POWER

Because of the three channels are identical it's possible to limit out consideration to one channel only.

It's possible to calculate the power dissipated by the device substracting the dissipation of external components from the power absorbed by the power supply.

The absorbed power is given by:

$$P_{abs} = V_{HT}\ I_{HT} + V_S\ I_S$$

With good approximation we can consider only the component due to high tension.

$$P_{abs} = V_{HT}\ (I1 + I2\ I_G)$$

Being $I_G << I1, I2$ we have:

$$P_{abs} = V_{HT}\ (I1 + I2)$$

with:

$$I1 = \frac{V_{HT} - V_{OBL}}{R1}$$

and:

$$I2 = \frac{V_{OBL} - (V_{REF} + 2V_{BE})}{R_f} \simeq \frac{V_{OBL}}{R_f}$$

where V_{OBL} is the black level at the output.

So:

$$P_{ads} = V_{HT} \left(\frac{V_{HT} - V_{OBL}}{R1} + \frac{V_{OBL}}{R_f} \right)$$

The power dissipated by external components is the dissipation due to R_f and R_B.

$$P_{est} = \frac{V_{Rf}^2}{R_f} + \frac{V_B^2}{R_B}$$

where:

$$V_{Rf} \simeq V_{OBL} - (V_{REF} + 2\,V_{BE}) \;\&\; V_{OBL}$$

$$V_B \simeq V_{REF} + 2\,V_{BE}$$

We have:

$$P_{est} = \frac{V_{OBL}^2}{R_f} + \frac{(V_{REF} + 2\,V_{BE})^2}{R_B}$$

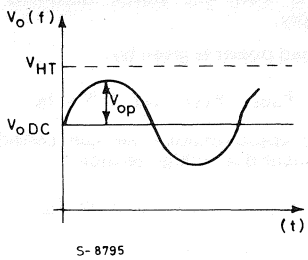
The statistically dissipated power for one channel is in conclusion:

$$P_S = V_{HT} \left(\frac{V_{HT} - V_{OBL}}{R1} + \frac{V_{OBL}^2}{R_f} \right) - \frac{V_{OBL}^2}{R_f} - \frac{(V_{REF} + 2\,V_{BE})^2}{R_B}$$

DINAMIC POWER

With an input sinusoidal signal the outptut signal is, as shown in fig. 15.

Fig. 15 - Output signal with a sinusoidal input



$$V_{o(t)} = V_{OBL} + V_{op} \sin\omega t$$

The current in the load capacitance C_L is given by:

$$i_{L(t)} = \omega\, C_L\, V_{op} \sin\omega t$$

The instantaneous power absorbed from the power supply is thus so given by:

$$p(t) = V_{HT} \cdot \omega\, C_L\, V_{op} \sin\omega t$$

This power is furnished only during half period, that is during the positive going output signal. The absorbed mean power is so:

$$P_{abs} = \frac{1}{2\pi} \int_0^{\pi} \omega\, C_L\, V_{HT}\, V_{op} \sin\omega t\, d(\omega t) =$$

$$= \frac{\omega\, C_L\, V_{HT}\, V_{op}}{2\pi} \left[-\cos\omega t \right]_0^{\pi} = 2\,f\,C_L\,V_{op}\,V_{HT}$$

The dynamically dissipated power is given by:

$$P_{diss} = \frac{V_{op}^2}{2\,R_f}$$

But during the horizontally flyback time and during vertical blanching, that is the 20% of the period, the cathodes are forced to int. off. so:

$$P_{ass} = 0{,}8 \cdot 2\,f\,C_L\,V_{op}\,V_{HT}$$

$$P_{diss} = 0{,}8 \cdot \frac{V_{op}^2}{2\,R_f}$$

If we consider now the total dissipated power for the three channels can write:

$$P_d = 3\,V_{HT} \cdot \left[\frac{V_{HT} - V_{OBL}}{R1} + \frac{V_{OBL}}{R_f} + 0{,}8 + 0{,}8\,(2\,f\,C_L\,V_{op}) \right] - 3 \left[\frac{V_{OBL}^2}{R_f} + \frac{(V_{REF} + 2\,V_{BE})^2}{R_B} + 0{,}8\,\frac{V_{op}^2}{2\,R_f} \right]$$

Considering the case:

$R1 = 21K\Omega$
$R_f = 68K\Omega$
$R_B = 1.8K\Omega$
$C_L = 10pF$
$V_{HT} = 200V$
$V_{OBL} = 150V$
$V_{op} = 40V$
$f = 4MHz$

the total dissipated power is:

$$P_{tot} = 3.25W$$

In this case, with a maximum room temperature of 70°C and a maximum junction temperature of 150°C a heatsink is required with thermal resistance of 20°C/W.

However the calculation performed above is clearly referred to the worst conditions. The use of this heatsink allows to work with a sufficient safety margin.